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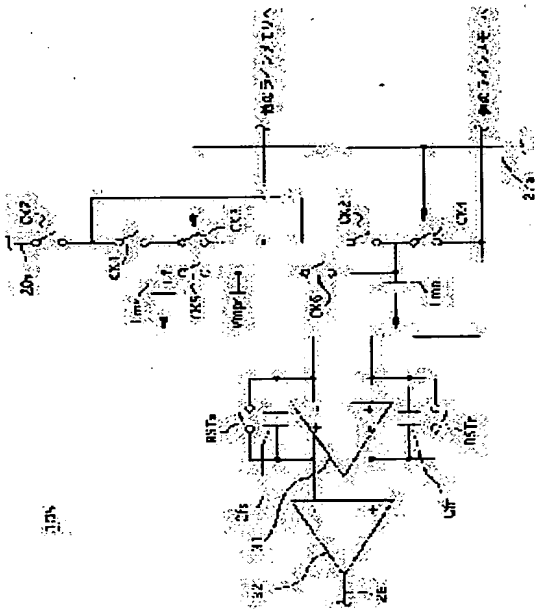
(54) SOLID-STATE IMAGE PICKUP DEVICE AND ITS DRIVE METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To suppress the influence of variance of sub-threshold current and to reduce the modulation variance of output voltage.
SOLUTION: A solid-state image pickup device accumulates the light emission electric charge in a high density embedded layer formed under a channel and modulates the threshold voltage to detect an optical signal, and a signal output circuit 105 outputs the difference voltage between a 1st source potential that undergone the light modulation and a 2nd source potential that undergone no light modulation yet. The circuit 105 has a 1st line memory Lms which is connected to a source area via a 1st switch CK1 and a 2nd line memory Lmn which is connected to the source area via a 2nd switch CK2 and also has a 1st high voltage block switch CK7 between both switches CK1 and CK2 and the source area.



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CLAIMS

[Claim(s)]

[Claim 1] It has the unit pixel equipped with the insulated gate field effect transistor for lightwave signal detection which adjoins light-receiving diode and this light-receiving diode. It has the high concentration buried layer which accumulates the optical generating charge generated by optical exposure for said light-receiving diode formed in the field. the part of said insulated gate field effect transistor -- a near source field -- it is -- the well under a gate electrode -- The solid state image sensor which accumulates said optical generating charge in said high concentration buried layer, is made to modulate threshold voltage, and detects a lightwave signal, The vertical-scanning signal drive scanning circuit which outputs a scan signal to the gate electrode of said insulated gate field effect transistor for lightwave signal detection, The high-pressure-distribution circuit which supplies the electrical potential difference for sweeping out said optical generating charge accumulated in said high concentration buried layer to the source field of said insulated gate field effect transistor, The 1st source potential in the condition of having accumulated said optical generating charge in said high concentration buried layer is inputted into the 1st input. The 2nd source potential in the condition of having swept out said optical generating charge from said high concentration buried layer is inputted into the 2nd input. The solid state camera characterized by having the switching circuit for a high-voltage block which has the signal output circuit which outputs the electrical potential difference corresponding to those inputs, and prevents the input of the high voltage from said high-pressure-distribution circuit in the preceding paragraph of said signal output circuit.

[Claim 2] The swicthed capacitor circuit where said signal output circuit has the 1st memory, the 2nd memory, the 1st switching circuit, the 2nd switching circuit, the 3rd switching circuit, the 4th switching circuit, and said 1st operational amplifier, It has the

operation amplifying circuit which has the 2nd operational amplifier. Said 3rd operational amplifier Have forward, forward [a negative input terminal and forward], and a negative output terminal, and a feedback capacitor (Cfs) is connected between said negative input terminals and said forward output terminals. A feedback capacitor (Cfn) is connected between said plus input terminals and said negative output terminals. And said 4th operational amplifier Have forward and a negative input terminal, and an output terminal, and negative [said] and a plus input terminal are connected to forward [of said 3rd operational amplifier], and a negative output terminal, respectively. Transmit said 1st source potential alternatively by said 1st switching circuit, and said 1st memory is made to memorize. Said 1st source potential is made to input into the negative input terminal of said 3rd operational amplifier alternatively from said 1st memory by said 3rd switching circuit. Transmit said 2nd source potential alternatively by said 2nd switching circuit, and the 2nd memory is made to memorize. Said 2nd source potential is made to input into the plus input terminal of said 3rd operational amplifier alternatively from said 2nd memory by said 4th switching circuit. Said 1st source potential is made to input into the negative input terminal of said 4th operational amplifier from the forward output terminal of said 3rd operational amplifier. And the solid state camera according to claim 1 characterized by making said 2nd source potential input into the plus input terminal of said 4th operational amplifier from the negative output terminal of said 3rd operational amplifier.

[Claim 3] The 1st swicthed capacitor circuit where said signal output circuit has the 1st memory, the 1st switching circuit, the 3rd switching circuit, and the 3rd operational amplifier, The 2nd memory, the 2nd switching circuit, the 4th switching circuit, and the 2nd swicthed capacitor circuit that has the 4th operational amplifier, Have an operation amplifying circuit, transmit said 1st source potential alternatively by said 1st switching circuit, and said 1st memory is made to memorize. Said 1st source potential is alternatively transmitted to the input terminal of said 3rd operational amplifier from said 1st memory by said 3rd switching circuit. Transmit said 2nd source potential alternatively by said 2nd switching circuit, and the 2nd memory is made to memorize. Said 2nd source potential is alternatively transmitted to the input terminal of said 4th operational amplifier from said 2nd memory by said 4th switching circuit. The solid state camera according to claim 1 characterized by inputting into said operation amplifying circuit said 1st and 2nd source potentials outputted from said 3rd and 4th operational amplifiers, and outputting the electrical potential difference of the difference of said 1st and 2nd source potentials.

[Claim 4] Said solid state camera is a solid state camera according to claim 2 or 3 characterized by having the video-signal output terminal further connected to the output of the drain electrical-potential-difference drive scanning circuit which supplies a drain electrical potential difference to the drain field of said insulated gate field effect transistor, the horizontal scanning signal input scanning circuit which supplies the signal which controls closing motion of the 3rd and 4th switching circuits of said signal output circuit, and said signal output circuit.

[Claim 5] Claim 2 characterized by connecting to said the 1st memory and said 2nd memory a means to impress a presetting electrical potential difference, respectively thru/or a solid state camera given in any 1 of 4.

[Claim 6] Said the 1st switching circuit and said 2nd switching circuit are [both] claim 2 characterized by a p channel MOS transistor and an n channel MOS transistor being the transmission gates by which parallel connection was carried out thru/or a solid state camera given in any 1 of 5.

[Claim 7] They are claim 2 which wiring branches from said source field, is connected with said the 1st switching circuit and said 2nd switching circuit, and is characterized by preparing said switching circuit for a high-voltage block between [one] said source fields and branch points of said wiring thru/or a solid state camera given in any 1 of 6.

[Claim 8] Said switching circuit for a high-voltage block consists of the 1st switching circuit for a high-voltage block, and the 2nd switching circuit for a high-voltage block. Wiring branches from said source field and it is connected with said the 1st switching circuit and said 2nd switching circuit. Said 1st switching circuit for a high-voltage block is prepared between the junction of said wiring, and said 1st switching circuit. Said 2nd switching circuit for a high-voltage block is claim 2 characterized by being prepared between said junction and said 2nd switching circuit thru/or a solid state camera given in any 1 of 6.

[Claim 9] The said switching circuit for high-voltage block, said 1st, and 2nd switching circuits for a high-voltage block are solid state cameras according to claim 7 or 8 characterized by being the MOS transistor of a depletion type.

[Claim 10] It has the unit pixel equipped with the insulated gate field effect transistor for lightwave signal detection which adjoins light-receiving diode and this light-receiving diode. It has the high concentration buried layer which accumulates the optical generating charge generated by optical exposure for said light-receiving diode formed in the field. the part of said insulated gate field effect transistor -- a near source field -- it is -- the well under a gate electrode -- The solid state camera which has the solid state image sensor which accumulates said optical generating charge in said high

concentration buried layer, is made to modulate threshold voltage, and detects a lightwave signal is used. The are recording period which stores up the optical generating charge generated by optical exposure in said high concentration buried layer for said light-receiving diode, The read-out period which reads the lightwave signal based on the optical generating charge accumulated in said high concentration buried layer, Are the drive approach of the solid state camera which repeats the initialization period which discharges the optical generating charge which remains to said high concentration buried layer in this order, and reads a lightwave signal, and it sets at the aforementioned read-out period. After accumulating an optical generating charge in said high concentration buried layer, the 1st memory is made to memorize the 1st source potential outputted from the source field of said insulated gate field effect transistor. Subsequently In said initialization period, after making connectionless between said source field and said 1st memory and between said source field and said 2nd memory The optical generating charge which impressed the electrical potential difference to said source field, and was accumulated in said high concentration buried layer is made to discharge. Subsequently The 2nd memory is made to memorize the 2nd source potential outputted from the source field of said insulated gate field effect transistor before said are recording period. Subsequently The drive approach of the solid state camera characterized by reading the 1st and 2nd source potentials which said 1st and 2nd memory was made to memorize in said are recording period, and outputting the electrical potential difference of the difference of said 1st source potential and said 2nd source potential.

[Claim 11] It has the unit pixel equipped with the insulated gate field effect transistor for lightwave signal detection which adjoins light-receiving diode and this light-receiving diode. It has the high concentration buried layer which accumulates the optical generating charge generated by optical exposure for said light-receiving diode formed in the field. the part of said insulated gate field effect transistor -- a near source field -- it is -- the well under a gate electrode -- The solid state camera which has the solid state image sensor which accumulates said optical generating charge in said high concentration buried layer, is made to modulate threshold voltage, and detects a lightwave signal is used. The are recording period which stores up the optical generating charge generated by optical exposure in said high concentration buried layer for said light-receiving diode, The read-out period which reads the lightwave signal based on the optical generating charge accumulated in said high concentration buried layer, Are the drive approach of the solid state camera which repeats the initialization period which discharges the optical generating charge which remains to said high

concentration buried layer in this order, and reads a lightwave signal, and it sets at the aforementioned read-out period. After accumulating an optical generating charge in said high concentration buried layer and making the 1st memory memorize a presetting electrical potential difference, said 1st memory is made to memorize the 1st source potential outputted from the source field of said insulated gate field effect transistor. Subsequently In said initialization period, after making connectionless between said source field and said 1st memory and between said source field and said 2nd memory The optical generating charge which impressed the electrical potential difference to said source field, and was accumulated in said high concentration buried layer is made to discharge. Subsequently Before said are recording period, after making the 2nd memory memorize a presetting electrical potential difference, make said 2nd memory memorize the 2nd source potential outputted from the source field of said insulated gate field effect transistor, next it sets to said are recording period. The drive approach of the solid state camera characterized by reading the 1st and 2nd source potentials which said 1st and 2nd memory was made to memorize, and outputting the electrical potential difference of the difference of said 1st source potential and said 2nd source potential.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the solid state camera using MOS mold image sensors and its drive approach of the threshold voltage modulation technique used for a video camera, an electronic camera, an image input camera, a scanner, or facsimile in more detail about a solid state camera and its drive approach.

[0002]

[Description of the Prior Art] Since semi-conductor image sensors, such as CCD mold image sensors and MOS mold image sensors, are excellent in mass-production nature, they are applied to almost all images input device equipment with progress of the detailed-ized technique of a pattern. MOS mold image sensors are improved taking advantage of the advantage that power consumption is small and can create a sensor component and a circumference circuit element by the same CMOS technology especially in recent years compared with CCD mold image sensors.

[0003] In view of the trend of such a world, the applicant for this patent improved MOS mold image sensors, performed patent application (Japanese Patent Application No. No. 186453 [ten to]) about the sensor component which has a carrier pocket (high concentration buried layer) under a channel field, and has acquired the patent (registration number No. 2935492). These MOS mold image sensors have circuitry shown in patent (registration number No. 2935492) drawing 8 (a), and in that actuation, as similarly shown in drawing 8 (b), they pass through an initialization period-are recording period-read-out period. Each electrode is made to impress and depletion-ize high reverse voltage at an initialization period, and the optical generating electron hole which remains in the hole pocket 25 is made to emit. Make an are recording period produce an optical generating electron hole by optical exposure, it is made to accumulate in the hole pocket 25, and the lightwave signal which is proportional to the accumulated dose of an optical generating electron hole at a read-out period is detected.

[0004] By invention concerning this patent (registration number No. 2935492), as shown in drawing 11 (a) of this application, and (b), in the combination of the MOS transistor for lightwave signal detection, and active loads, such as a constant current source established outside, the impedance of a signal is lowered by the source follower, the memory space which does not detect and illustrate source potential is made to charge, and the voltage signal is outputted.

[0005]

[Problem(s) to be Solved by the Invention] However, a pixel is made detailed, if wiring width of face becomes thin, parasitism resistance will rise, and it becomes a problem as dispersion in the voltage drop in wiring by series resistance, and between wiring. Then, since the ratio occupied to the source current of the subthreshold level current (property in front of the standup of the drain current in a drain electrical-potential-difference-drain current characteristic) by drain induction barrier fall (DIBL) will increase relatively and output voltage will be governed by the subthreshold level current when channel length is short if a current value is decreased in order to control a part for a voltage drop, dispersion in the modulation of output voltage increases.

[0006] This invention is created in view of the trouble of the above-mentioned conventional technique, controls the effect of dispersion in a subthreshold level current, and offers the solid state camera which can reduce modulation dispersion of output voltage, and its drive approach.

[0007]

[Means for Solving the Problem] In order to solve the above-mentioned technical

problem, this invention relates to a solid state camera, and as shown in drawing 1 , it has each unit pixel 101 containing the insulated gate field effect transistor 112 for lightwave signal detection (MOS transistor) which adjoins the light-receiving diode 111 and the light-receiving diode 111 as that basic configuration. the well which connected the light-receiving diode 111 and MOS transistor 112 mutually in each unit pixel 101 -- it forms in Fields 15a and 15b -- having -- the well of the periphery of the source field of MOS transistor 112 -- it is characterized by having the high concentration buried layer (carrier pocket) 25 which accumulates an optical generating charge into field 15b.

[0008] The gate electrode of MOS transistor 112 was connected to the vertical-scanning signal (VSCAN) drive scanning circuit 102, and the source field is connected with the signal output circuit 105 through a perpendicular output line. And as shown in drawing 2 , a source field is directly linked with the 1st Rhine memory (the 1st memory) Lms and the 2nd Rhine memory (the 2nd memory) Lmn which consist of a capacitor in the above-mentioned signal output circuit 105, and it is characterized by not having active loads, such as a constant current source. Furthermore, it has one or two swicthed capacitor circuits in the signal output circuit 105, and is characterized by having composition which outputs the electrical potential difference of the difference of the source potential after the light modulation memorized by the 1st and 2nd Rhine memory Lms and Lmn through this swicthed capacitor circuit, and the source potential in front of light modulation.

[0009] Furthermore, the detail of the above-mentioned signal output circuit 105 is shown in drawing 2 . As shown in drawing 2 , perpendicular output line 20a linked to the source field of MOS transistor 112 for lightwave signal detection branched, one connected with the end child of the 1st Rhine memory Lms who memorizes the electrical potential difference which contains a lightwave signal electrical potential difference and noise voltage through 1st switching circuit CK1, and others have connected with the end child of the 2nd Rhine memory Lmn who memorizes noise voltage through 2nd switching circuit CK2.

[0010] And the preceding paragraph of the signal output circuit 105 is equipped with the switching circuit for a high-voltage block which prevents the input of the high voltage from the high-pressure-distribution circuit 108. That is, it is between 1st switching circuit CK1 and 2nd switching circuit CK2, and the source field of MOS transistor 112 for lightwave signal detection, and is characterized by to have one switching circuit CK7 for a high-voltage block on perpendicular output line 20a, or having the 1st and 2nd switching circuits CK8 and CK9 for a high-voltage block, respectively, in [branching wiring from perpendicular output line 20a].

[0011] In this case, it is characterized by both 1st switching circuit CK1 and 2nd switching circuit CK2 being the transmission gates where parallel connection of a p channel MOS transistor and the n channel MOS transistor was carried out. Moreover, the end child of the 1st Rhine memory Lms connected with the negative input terminal of an operational amplifier (the 3rd operational amplifier) 31 through 3rd switching circuit CK3 controlled by HSCAN supply line 27a, and the end child of the 2nd Rhine memory Lmn has connected with the plus input terminal of the 1st operational amplifier 31 through 4th another switching circuit CK4 controlled by HSCAN supply line 27a. Furthermore, the forward output terminal of the 1st operational amplifier 31 is connected to the negative input terminal of the 2nd operation amplifying circuit 32, and the negative output terminal of the 1st operational amplifier 31 is connected to the plus input terminal of the 2nd operation amplifying circuit 32. The output terminal of the 2nd operation amplifying circuit 32 is connected to the video-signal output terminal 107 through the water Hiraide line of force 26. In addition, although the 1st and 2nd swicthed capacitor circuits were unified by the 1st one operational amplifier 31 and the configuration of one swicthed capacitor circuit is taken above, you may divide into two swicthed capacitor circuits, the 1st and the 2nd, using the 3rd and 4th operational amplifiers.

[0012] Moreover, a means to impress a presetting electrical potential difference is connected to the 1st and 2nd Rhine memory Lms and Lmn. The are recording period which stores up the optical generating carrier generated by optical exposure in a high concentration buried layer in the drive approach of this invention using the above-mentioned solid state camera, The read-out period which reads the lightwave signal based on the optical generating carrier accumulated in the high concentration buried layer, Are the drive approach of the solid state camera which repeats the initialization period which discharges the optical generating carrier which remains to a high concentration buried layer in this order, and reads a lightwave signal, and it sets at a read-out period. After accumulating an optical generating carrier in a high concentration buried layer, the 1st Rhine memory is made to memorize the 1st source potential in which the MOS transistor for lightwave signal detection carried out a source field sky output. Subsequently In an initialization period, after making connectionless both between a source field and the 1st Rhine memory and between a source field and the 2nd Rhine memory The optical generating charge which impressed the electrical potential difference to the source field, and was accumulated in the high concentration buried layer is made to discharge. Subsequently The 2nd source potential outputted from the source field of the MOS transistor for lightwave signal detection

before the are recording period is made to memorize. Subsequently The 1st and 2nd source potentials which the 1st and 2nd Rhine memory was made to memorize are read, and the electrical potential difference of the difference of the 1st source potential and the 2nd source potential is outputted.

[0013] Since the MOS transistor for lightwave signal detection of the threshold modulation mold which prepares a high concentration buried layer in the bottom of a channel, and accumulates an optical generating carrier in the bottom of a channel as an MOS transistor for lightwave signal detection in a pixel is used according to above-mentioned this invention, the channel length is long. For this reason, since the electric field from a drain field are also eased, a drain induction barrier fall (DIBL) is controlled. Therefore, since the threshold shift is small, as a result fluctuation of a subthreshold level current is also small, the charging current can be minimized. Thereby, since the potential fall by parasitism resistance of wiring etc. can be controlled, direct connection with a capacitive load is attained.

[0014] Moreover, although the time amount of finite is needed for the writing to the Rhine memory, the write-in time amount to the Rhine memory is sharply short as compared with a blanking period or a read-out period. For this reason, the writing to the Rhine memory can be performed between blanking periods etc. By the way, although it will go into the Rhine memory which those parasitic capacitance should read at juxtaposition if two or more Rhine memory is arranged in juxtaposition, the 1st and 2nd source potentials which the Rhine memory which should be read was made to memorize are outputted through a swicthed capacitor circuit. At this time, in a swicthed capacitor circuit, since charge transfer is performed by the operational amplifier 31, the parasitic capacitance seen from the output side of a swicthed capacitor circuit becomes small. For this reason, it reads, even if it arranges two or more memory devices in juxtaposition, and a rate is hardly influenced. Moreover, since the effect of parasitic capacitance is small, there is also an advantage that the maximum gain is acquired.

[0015] Moreover, by connecting to the 1st and 2nd Rhine memory a means to impress a presetting electrical potential difference The presetting electrical potential difference higher [than touch-down potential] and lower than the source potential made to memorize before making the 1st and 2nd Rhine memory memorize source potential is made to memorize. By this Also while impressing touch-down potential to the gate electrode of the MOS transistor for lightwave signal detection, actuation of the MOS transistor for lightwave signal detection can be suppressed certainly, and leakage current can be controlled.

[0016] Moreover, it is distorted and enables it to let a higher signal level pass that there

is nothing by using the transmission gate where parallel connection of a p channel MOS transistor and the n channel MOS transistor was carried out as [both] the 1st switching circuit and 2nd switching circuit. Since bias of the pn junction of the source / drain field of one transistor is carried out to the forward direction among the CMOS transistors which constitute a transmission gate, a transmission gate stops in this case, operating normally, if the high electrical potential difference for initialization is impressed to the source field of the MOS transistor for lightwave signal detection.

[0017] In order to prevent this, it is between the 1st switching circuit and the 2nd switching circuit, and the source field of the MOS transistor for lightwave signal detection, and one switching circuit for a high-voltage block is put in on the perpendicular output line. Or the 1st and 2nd switching circuits for a high-voltage block are put in, respectively between the 1st switching circuit and the source field of the MOS transistor for lightwave signal detection, and between the 2nd switching circuit and the source field of the MOS transistor for lightwave signal detection. Such a problem can be prevented by making connectionless both between the 1st switching circuit and source fields and between the 2nd switching circuit and source fields at the initialization period which impresses the high electrical potential difference for making by this the optical generating charge accumulated in the high concentration buried layer sweep out.

[0018] in addition, a well -- when a field etc. is a conductivity type contrary to the above (i.e., when a high concentration buried layer is n mold), a high concentration buried layer serves as an electron pocket (carrier pocket), and will accumulate an optical generating electron.

[0019]

[Embodiment of the Invention] Below, it explains, referring to a drawing about the gestalt of operation of this invention. Drawing 8 is the top view showing the component layout in the unit pixel of the MOS mold image sensors concerning the gestalt of operation of this invention. As shown in drawing 8 , the light-receiving diode 111 and MOS transistor 112 for lightwave signal detection are adjoined and formed in the unit pixel 101. In addition, the thing of the MOS transistor for lightwave signal detection may only be hereafter called MOS transistor 112. As MOS transistor 112, the n channel MOS (nMOS) which has low concentration drain structure (LDD structure) is used.

[0020] the well from which these light-receiving diode 111 and MOS transistor 112 differ, respectively -- a field, i.e., the 1st well, -- field 15a and the 2nd well -- it forms in field 15b -- having -- those wells -- Fields 15a and 15b are connected mutually. the 1st well of the part of the light-receiving diode 111 -- field 15a constitutes a part of generating field

of the charge by optical exposure. the 2nd well of the part of MOS transistor 112 -- field 15b constitutes the gate field to which the threshold voltage of a channel can be changed with the potential given to this field 15b.

[0021] The part of MOS transistor 112 has low concentration drain (LDD) structure. The drain fields 17a and 17b are formed so that the periphery section of the ring-like gate electrode 19 may be surrounded, and the source field 16 is formed so that it may be surrounded by the inner circumference of the ring-like gate electrode 19. The impurity range 17 of the light-receiving diode 111 which low-concentration drain field 17a extends, and has the almost same high impurity concentration as low-concentration drain field 17a is formed. namely, the 1st and 2nd wells which connected mutually an impurity range 17 and low-concentration drain field 17a -- it is formed in one so that most fields may start the surface of Fields 15a and 15b. Moreover, high-concentration drain field 17b as a contact layer is formed so that a light sensing portion may be avoided to the outside periphery of an impurity range 17 and low-concentration drain field 17a and it may connect with low concentration drain field 17a.

[0022] furthermore, the carrier pocket (high concentration buried layer) 25 which is the description of these MOS mold image sensors -- the 2nd well under the gate electrode 19 -- it is in field 15b, and it is formed so that the source field 16 may be surrounded in the periphery of the source field 16. The drain fields 17a and 17b are connected with the drain electrical-potential-difference (VDD) supply line (or drain electrode) 22 through contact layer 17b of low resistance, the gate electrode 19 is connected to the vertical-scanning signal (VSCAN) supply line 21, and the source field 16 is connected to the perpendicular output line (or source electrode) 20.

[0023] Moreover, fields other than light-receiving aperture 24 of the light-receiving diode 111 are shaded by the metal layer (light-shielding film) 23. It sets in the component actuation for the lightwave signal detection in the above-mentioned MOS mold image sensors, and is an are recording period-read-out period-initialization period (**** period)-are recording period. - A series of processes of an are recording period-read-out period-initialization period (**** period) are repeated like .. In addition, with the gestalt of this operation, the blanking period is established between the initialization period (**** period) and the are recording period.

[0024] in an are recording period, a carrier is generated by optical exposure -- making -- the inside of a carrier -- an electron hole (hole) -- the 1st and 2nd wells -- the inside of field 15a and 15b is moved, and it is made to accumulate in the carrier pocket 25 While impressing the forward electrical potential difference of +2-3V to the drain fields 17a and 17b about, a low forward or negative electrical potential difference to which MOS

transistor 112 maintains a cut-off condition to the gate electrode 19 is impressed. This are recording period is also a period to which the electrical potential difference of a difference with the 2nd source potential before the 1st source potential and lightwave signal which were modulated with the lightwave signal made to memorize, respectively go into the 1st and 2nd Rhine memory (the 1st and 2nd memory) is made to output.

[0025] Change of the threshold voltage of MOS transistor 112 by the optical generating charge accumulated in the carrier pocket 25 is read as change of source potential, and the 1st Rhine memory is made to memorize in a read-out period. While impressing the forward electrical potential difference of +2-3V to the drain fields 17a and 17b about so that MOS transistor 112 may operate by the saturation state, the forward electrical potential difference of +2-3V is about impressed to the gate electrode 19.

[0026] In an initialization period, before accumulating an optical generating charge (optical generating carrier), an electron hole, an electron, etc. which carbonate an optical generating charge, an acceptor, a donor, etc. to whom read-out finishes and remains, or are captured by surface level discharge the residual charge before read-out of a lightwave signal out of a semi-conductor, and empty the carrier pocket 25. The about [7-8V] forward high voltage is usually impressed to the source field 16, the drain fields 17a and 17b, or the gate electrode 19 more than abbreviation +5V.

[0027] It is a period required for a cuff of the horizontal scanning prepared between the initialization period and the are recording period, and the 2nd Rhine memory is made to memorize the 2nd source potential in the condition of having swept out the optical generating charge from the carrier pocket 25 using this period, in a blanking period. Next, the device structure of the MOS mold image sensors concerning the gestalt of operation of this invention is explained using a sectional view.

[0028] Drawing 9 (a) is the sectional view showing the device structure of the MOS mold image sensors concerning the gestalt of operation of this invention equivalent to the sectional view which meets the A-A line of drawing 8 . Drawing 9 (b) is drawing showing the situation of potential along a semi-conductor substrate front face. As shown in drawing 9 (a), on the high-impurity-concentration 1x substrate 11 which consists of three or more [1018cm -] p-type silicon, 3 about [1x1015cm high impurity concentration to] n mold silicon is grown epitaxially, and an epitaxial layer 12 is formed.

[0029] Two or more formation of the unit pixel 101 which contains the light-receiving diode 111 and MOS transistor 112 for lightwave signal detection in this epitaxial layer 12 is carried out. And the field insulator layer (isolation insulator layer) 14 is formed in epitaxial layer 12 front face between the adjoining unit pixels 101 of selective oxidation (LOCOS) so that each unit pixel 101 may be separated. Furthermore, it is the lower part

of the field insulator layer 14, and the component isolation region 13 of p mold is formed so that the epitaxial layer 12 of n mold may be divided into the substrate 11 upper part, including the whole interface of an epitaxial layer 31 and the field insulator layer 14.

[0030] Next, drawing 9 (a) explains the detail of the light-receiving diode 111. The light-receiving diode 111 consists of surfaces of 1st well field 15a of p mold formed in the epitaxial layer 12 and the surface of an epitaxial layer 12, and 1st well field 15a in the impurity range 17 of n mold which extends on the surface of an epitaxial layer 12.

[0031] The impurity range 17 is formed so that it may extend from low-concentration drain field 17a of MOS transistor 112 for lightwave signal detection which has low concentration drain (LDD) structure. In the are recording period which gave [above-mentioned] explanation, it connects with the drain electrical-potential-difference supply line 22, and bias of the impurity range 17 is carried out to electropositive potential. this time -- an impurity range 17 and the 1st well -- an interface with field 15a to a depletion layer -- the 1st well -- the whole field 15a is reached at the epitaxial layer 12 of breadth and n mold. on the other hand -- the interface of a substrate 11 and an epitaxial layer 12 to a depletion layer -- an epitaxial layer 12 -- breadth and the 1st well -- field 15a is reached.

[0032] the 1st well -- since field 15a and an epitaxial layer 12 are connected with gate field 15b of MOS transistor 112, they can use effectively these holes generated by light as a charge for the threshold voltage modulation of MOS transistor 112. if it puts in another way -- the 1st well -- field 15a and the epitaxial layer 12 whole serve as a carrier generating field by light.

[0033] Moreover, the light-receiving diode 111 has the embedded structure to the electron hole (hole) generated by light in that the carrier generating field by light is arranged under an impurity range 17 in the above-mentioned light-receiving diode 111. Therefore, it is not influenced by the semi-conductor layer front face with many trapping levels, but reduction of a noise can be aimed at. Next, drawing 9 (a) explains the detail of MOS transistor 112 for lightwave signal detection.

[0034] the 2nd well of p mold with which MOS transistor 112 part was formed sequentially from the bottom in the substrate 11 of p mold, the epitaxial layer 12 of n mold formed on this substrate 11, and this epitaxial layer 12 -- it has field 15b. This MOS transistor 112 has the structure where low-concentration drain field 17a of n mold surrounds the periphery of the ring-like gate electrode 19. Low-concentration drain field 17a of n mold is formed in one with the impurity range 17 of n mold. It connects with this impurity range 17, and high-concentration drain field 17b prolonged even in the component isolation region 13 and the isolation insulator layer 14 is formed in the

outside periphery of the impurity range 17 which extends from low-concentration drain field 17a. High-concentration drain field 17b becomes the contact layer of the drain electrode 22.

[0035] Moreover, the source field 16 of n mold is formed so that it may be surrounded with the ring-like gate electrode 19. The center section serves as high concentration and, as for the source field 16, the periphery serves as low concentration. The source electrode 20 is connected to the source field 16. the gate electrode 19 -- the 2nd well between drain field 17a and the source field 16 -- it is formed through gate dielectric film 18 on field 15b. the 2nd well under the gate electrode 19 -- the surface of field 15b serves as a channel field. Furthermore, in the usual operating voltage, in order to hold a channel field in a reversal condition or the DEPURESHON condition, n mold impurity of the suitable concentration for a channel field is introduced, and channel dope layer 15c is formed.

[0036] the 2nd well under the channel field -- it is in field 15b, the direction of channel length is the periphery of a field 16, i.e., a source field, a part, and the source field 16 is surrounded -- as -- p+ The carrier pocket (high concentration buried layer) 25 of a mold is formed. This p+ The carrier pocket 25 of a mold can be formed with ion-implantation. the 2nd well below the channel field which produces the carrier pocket 25 on a front face -- it is formed in field 15b. As for the carrier pocket 25, forming so that a channel field may not be started is desirable.

[0037] Above-mentioned p+ In the carrier pocket 25 of a mold, since the potential over an optical generating hole becomes low among optical generating charges, when an electrical potential difference higher than gate voltage is impressed to the drain fields 17a and 17b, an optical generating hole can be brought together in this carrier pocket 25. An optical generating hole is accumulated in the carrier pocket 25 at drawing 9 (b), and the potential Fig. in the condition that induction of the electron was carried out to the channel field, and the reversal field is generated is shown. The threshold voltage of MOS transistor 112 changes with these stored charge. Therefore, detection of a lightwave signal can be performed by detecting change of this threshold voltage.

[0038] by the way, the electric field which impress a high electrical potential difference to the gate electrode 19, and are produced by it in the initialization period of the above-mentioned carrier -- the 2nd well -- the carrier which remains in field 15b is swept out to the substrate 11 side. in this case, the impressed electrical potential difference -- channel dope layer 15c of a channel field, and the 2nd well -- an interface with field 15b to a depletion layer -- the 2nd well -- field 15b -- the interface of breadth and the substrate 11 of p mold, and an epitaxial layer 12 to a depletion layer -- the 2nd

well -- it spreads in the epitaxial layer 12 under field 15b. therefore, the range where the electric field by the electrical potential difference impressed to the gate electrode 19 reach -- mainly -- the 2nd well -- field 15b and the 2nd well -- the epitaxial layer 12 under field 15b is covered.

[0039] Next, with reference to drawing 1 , the configuration of the whole MOS mold image sensors using the unit pixel of the above-mentioned structure is explained. Drawing 1 shows the circuitry Fig. of the MOS mold image sensors in the gestalt of operation of this invention. As shown in drawing 1 , these MOS mold image sensors have taken the configuration of a two-dimensional array sensor, and the unit pixel 101 of the above-mentioned structure is arranged by the direction of a train, and the line writing direction in the shape of a matrix.

[0040] Moreover, the drive scanning circuit 102 of a vertical-scanning signal (VSCAN) and the drive scanning circuit 103 of a drain electrical potential difference (VDD) are arranged across the pixel field at the right and left. every one vertical-scanning signal supply lines 21a and 21b have come out from the drive scanning circuit 102 of a vertical-scanning signal (VSCAN) for every line. Each vertical-scanning signal supply lines 21a and 21b are connected to the gate of MOS transistor 112 in all the unit pixels 101 on a par with a line writing direction.

[0041] moreover, every one drain electrical-potential-difference supply lines (VDD supply line) 22a and 22b have come out from the drive scanning circuit 103 of a drain electrical potential difference (VDD) for every line. Each drain electrical-potential-difference supply lines (VDD supply line) 22a and 22b are connected to the drain of MOS transistor 112 for lightwave signal detection in all the unit pixels 101 on a par with a line writing direction. Moreover, different perpendicular output lines 20a and 20b for every train are formed, and each perpendicular output lines 20a and 20b are connected to the source of MOS transistor 112 in all the unit pixels 101 located in a line in the direction of a train, respectively.

[0042] Furthermore, the source field of MOS transistor 112 is connected with the signal output circuit 105 through a perpendicular output line for every train. And as shown in drawing 2 , the source field is directly linked with the Rhine memory which consists of an input capacitor in the above-mentioned signal output circuit 105. It is characterized by having not connected active loads, such as a constant current source, to a source field.

[0043] The video signal (Vout) which does not contain the noise component by residual charge which drove MOS transistor 112 of sequential ** each unit pixel 101, and is proportional to the amount of incidence of light with a vertical-scanning signal (VSCAN) and a horizontal scanning signal (HSCAN) is read from the signal output

circuit 105. The detail of the above-mentioned signal output circuit 105 is shown in drawing 2 . As shown in drawing 2 , perpendicular output line 20a linked to the source field of MOS transistor 112 for lightwave signal detection branches. One connects with the end child of the 1st Rhine memory Lms who memorizes the 1st source potential which contains a lightwave signal electrical potential difference and the noise voltage by the residual charge before are recording of an optical generating charge through 1st switching circuit CK1. Others have connected with the end child of the 2nd Rhine memory Lmn who memorizes only the above-mentioned noise voltage through 2nd switching circuit CK2. Furthermore, it has switching circuit CK7 for a high-voltage block on perpendicular output line 20a of the preceding paragraph of the signal output circuit 105, i.e., this side of a junction. Thereby, the high voltage from the pressure-up scanning circuit (high-pressure-distribution circuit) 108 explained later can prevent now being inputted into the signal output circuit 105 alternatively.

[0044] Moreover, the end child of the 1st Rhine memory Lms connected with the negative input terminal of the 1st operational amplifier 31 through 3rd switching circuit CK3 controlled by HSCAN supply line 27a, and the end child of the 2nd Rhine memory Lmn has connected with the plus input terminal of the 1st operational amplifier 31 through 4th another switching circuit CK4 controlled by HSCAN supply line 27a. Furthermore, the forward output terminal of the 1st operational amplifier 31 was connected to the negative input terminal of the 2nd operational amplifier 32, and the negative output terminal of the 1st operational amplifier 31 is connected to the plus input terminal of the 2nd operational amplifier 32. The output terminal of the 2nd operational amplifier 32 is connected to the video-signal output terminal 107 through the water Hiraide line of force 26.

[0045] Parallel connection of the feedback capacitor Cfs and the reset switch circuit RSTs is carried out between the negative input terminal of the 1st operational amplifier 31, and a forward output terminal, and parallel connection of the feedback capacitor Cfn and the reset switch circuit RSTn is carried out between the plus input terminal and the negative output terminal. Moreover, it has a circuit for impressing the presetting electrical potential difference Vmpr to the 1st and 2nd Rhine memory Lms and Lmn. Before making the 1st and 2nd Rhine memory Lms and Lmn memorize source potential by this, it is higher than touch-down potential, and the presetting electrical potential difference lower than the source potential made to memorize can be made to be able to memorize, also while impressing touch-down potential to the gate electrode 19 of the insulated gate field effect transistor 112 for lightwave signal detection, actuation of an insulated gate field effect transistor 112 can be suppressed certainly, and leakage

current can be controlled.

[0046] The 1st and 3rd switching circuits CK1 and CK3, the 1st Rhine memory Lms, and the 1st operational amplifier 31 of a part to which the feedback capacitor Cfs and the reset switch circuit RSTs were connected constitute the 1st swicthed capacitor circuit. Moreover, the 2nd and 4th switching circuits CK2 and CK4, the 2nd Rhine memory Lmn, and the 1st operational amplifier 31 of a part to which the feedback capacitor Cfn and the reset switch circuit RSTn were connected constitute the 2nd swicthed capacitor circuit. The reset switch circuits RSTs and RSTn are closed when removing the charge charged by the feedback capacitors Cfs and Cfn.

[0047] It is independent about an MOS transistor etc. so that circuit actuation explained to the gestalt of this operation as it was shown in drawing 3 in fact, although it is typically shown in a form like drawing 2 in order to show functionally that the switching circuits in the above-mentioned signal output circuit 105 (CK1 thru/or CK7, RSTs, RSTn) open and close an applicable wiring way may be performed appropriately, or it combines, and uses. Here, the so-called transmission gate where parallel connection of a p channel MOS transistor and the n channel MOS transistor was carried out as [both] 1st switching circuit CK1 and 2nd switching circuit CK2 is used, and also CK3 thru/or CK7 use the n channel MOS altogether.

[0048] The transmission gate which consists of a CMOS transistor as [both] 1st switching circuit CK1 and 2nd switching circuit CK2 is used, because it is distorted and can let a higher signal level pass that there is nothing. Moreover, as for n channel MOS in all, it is desirable for using the transmission gate to use the thing of a depletion type with a low threshold.

[0049] Although it is effective in sharing the 1st one operational amplifier 31 in the 1st and 2nd swicthed capacitor circuits, and reducing common mode noise by this with the gestalt of this operation, a separate operational amplifier (the 3rd and 4th operational amplifiers) may be formed by the case. In this case, although a separate operational amplifier has forward and a negative input terminal, respectively, the Rhine memory is connected to a negative input terminal among forward [in each operational amplifier], and a negative input terminal, and the direction of a plus input terminal is set to touch-down potential.

[0050] Moreover, it has the pressure-up scanning circuit (high-pressure-distribution circuit) 108, and each pressure-up voltage-output lines 30a and 30b from the pressure-up scanning circuit 108 are connected to each perpendicular output lines 20a and 20b. Namely, the electrical potential difference by which the pressure up was carried out is impressed to the source field of MOS transistor 112 of each unit pixel 101

for every train. The electrical potential difference by which the pressure up was carried out is further built over the gate as a result through the capacity between the gate-sources. thereby -- a well -- the field strength concerning a field can be increased, a carrier can sweep, and **** can be promoted.

[0051] Drawing 4 shows the timing chart of each I/O signal for operating the MOS mold image sensors concerning this invention. Moreover, drawing 5 shows the timing chart of each I/O signal in the signal output circuit 105 for operating the MOS mold image sensors concerning this invention. in this case, the 1st and 2nd wells of p mold -- using Fields 15a and 15b, when MOS transistor 112 for lightwave signal detection is nMOS, it applies.

[0052] Next, according to drawing 4 and drawing 5 , photodetection actuation of the solid state image sensor with which a single string continued is explained briefly. Photodetection actuation is performed by repeating a series of processes which consist of an are recording period-read-out period-initialization period (**** period), as described above. Here, explanation is begun from an are recording period for convenience' sake. First, in an are recording period, low gate voltage is impressed to the gate electrode 19 of MOS transistor 112 for lightwave signal detection, and the electrical potential difference (VDD) of the abbreviation 2-3V required for actuation of a transistor is impressed to the drain fields 17a and 17b. this time -- the 1st well -- field 15a and the 2nd well -- field 15b and an epitaxial layer 12 depletion-ize. At this time, the electric field which go to the source field 16 arise from the drain fields 17a and 17b.

[0053] And let the outgoing end of the pressure-up scanning circuit 108 be touch-down potential (for it to become the source potential of MOS transistor 112) in the are recording period in front of a read-out period. this time -- the outgoing end of the VSCAN drive scanning circuit 102 -- touch-down potential (it becomes the gate potential of MOS transistor 112) -- becoming -- **** -- the output (Vpdn) of the VDD drive scanning circuit 103 -- about 3.3 -- it is V.

[0054] Then, light is irradiated at the light-receiving diode 111, and an electronic-electron hole pair (optical generating charge) is produced. An optical generating hole is poured into gate field 15b of MOS transistor 112 for lightwave signal detection among this optical generating charge by the above-mentioned electric field, and it is accumulated in the carrier pocket 25. While the depletion-layer width of face which spreads in gate field 15b under it from a channel field is restricted by this, the potential of the source field 16 neighborhood is modulated, and the threshold voltage of MOS transistor 112 changes.

[0055] In addition, in an are recording period, although the electrical potential

difference of the difference of the source potential memorized by the Rhine memory Lms and Lmn is outputted to the video-signal output terminal 107, this actuation will be explained after a blanking period. Next, in the first half of a read-out period, while closing switching circuit CK7 for a high-voltage block, and opening 2nd switching circuit CK2 wide and making it flow through between 1st switching circuit CK1 and source fields, suppose un-flowing between the 2nd Rhine memory Lmn and source fields. Moreover, let the output (VPGn) of the VSCAN drive scanning circuit 102 be touch-down potential (for it to become the gate potential of MOS transistor 112). While closing 1st switching circuit CK1 of the signal output circuit 105 to coincidence, precharge switching circuit CK5 is closed to it, and it is made to memorize the presetting electrical potential difference Vmpr (1.6V (for it to become the source potential of MOS transistor 112)) in the 1st Rhine memory Lms. On the other hand, VDD drive scanning-line 22a is maintained at about 3.3 V.

[0056] Next, close switching circuit CK7 for a high-voltage block, and 2nd switching circuit CK2 is kept opened wide, and it is made to flow through between 1st switching circuit CK1 and source fields in the second half of a read-out period. the output (VPGn) of the VSCAN drive scanning circuit 102 -- about 2.2 -- it is referred to as V (it becomes the gate potential of MOS transistor 112). On the other hand, VDD drive scanning-line 22a is maintained at about 3.3 V (it becomes the drain potential of MOS transistor 112).

[0057] That is, the gate voltage of the abbreviation 2-3V to which MOS transistor 112 can operate by the saturation state is impressed to the gate electrode 19, and the electrical potential difference VDD which are the abbreviation 2-3V to which MOS transistor 112 can operate to the drain fields 17a and 17b is impressed. Thereby, the reversal field of low electric field is formed in a part of channel field of the carrier pocket 25 upper part, and a high electric-field field is formed in the remaining part of a channel field. At this time, the drain voltage-current property of MOS transistor 112 shows saturation characteristics, as shown in drawing 10 .

[0058] Thereby, as shown in drawing 5 (a), the 1st Rhine memory Lms is charged. And source potential will rise as charge progresses, and a drain current will not flow in the place where source potential became equal to threshold voltage. Thereby, charge is completed and the threshold voltage (source potential Vouts) by which light modulation was carried out to the 1st Rhine memory Lms is memorized. The electrical potential difference (that is, noise voltage (Voutn) is called.) which originated in the charge by the optical generating charge besides the electrical potential difference only by the optical generating charge is also included in this threshold voltage.

[0059] Disconnection of switching circuit CK7 for a high-voltage block opens the 1st

switching circuit CK1 and precharge switching circuit CK5 on a peach after termination of a read-out period. Next, it moves to initialization actuation. initialization actuation -- setting -- the inside of the carrier pocket 25, and the 1st and 2nd wells -- the charge which remains in field 15a and 15b is discharged. That is, by adding 6.6V to the source of MOS transistor 112 for lightwave signal detection from the pressure-up scanning circuit 108, potential of a drain is set to 6.6V through the capacity of MOS transistor 112 for lightwave signal detection, and, in addition to 2V already charged, potential of the gate electrode 19 is set to about 8.6V through the capacity between the source-gates.

[0060] the electrical potential difference impressed to the gate electrode 19 at this time -- the 2nd well -- field 15b and the 2nd well -- the epitaxial layer 12 under field 15b is started. the high electric field generated at this time -- the 2nd well -- a carrier can be certainly swept out from field 15b. Thus, a carrier can be more certainly swept out with low supply voltage by having the pressure-up scanning circuit 108.

[0061] Moreover, since switching circuit CK7 for a high-voltage block is opened wide, it is un-flowing between 1st switching circuit CK1 and a source field and between 2nd switching circuit CK2 and a source field. Therefore, those malfunction can be prevented, without impressing the high electrical potential difference for sweeping out a carrier to the source / drain field of the p channel MOS of the transmission gate which constitutes 1st switching circuit CK1 and 2nd switching circuit CK2.

[0062] After discharging the optical generating charge accumulated in the high concentration buried layer 25, while closing switching circuit CK7 for a high-voltage block, and opening the 1st switching circuit wide in the first half of the blanking period in front of an are recording period and making it flow through between 2nd switching circuit CK2 and source fields, suppose un-flowing between the 1st Rhine memory Lms and source fields. Moreover, the output (VPGn) of the VSCAN drive scanning circuit 102 is made into touch-down potential (it becomes the gate potential of MOS transistor 112), and the output (Vpdn) of the VDD drive scanning circuit 103 is set to 3.3V (it becomes the drain potential of MOS transistor 112) at coincidence. Moreover, precharge switching circuit CK6 and 2nd switching circuit CK2 are closed, and the 2nd Rhine memory Lmn is connected to the source field of an insulated gate field effect transistor 112. Thereby, the 2nd Rhine memory Lmn is made to memorize the presetting electrical potential difference Vmpr (1.6V (for it to become the source potential of MOS transistor 112)).

[0063] Next, close switching circuit CK7 for a high-voltage block, and 1st switching circuit CK1 is kept opened wide, and it is made to flow through between 2nd switching circuit CK2 and source fields in the second half of a blanking period. moreover, the

output (VPGn) of the VSCAN drive scanning circuit 102 -- about 2.2 -- it is referred to as V (it becomes the gate potential of MOS transistor 112). On the other hand, VDD drive scanning-line 22a is maintained at about 3.3 V.

[0064] Thereby, the reversal field of low electric field is formed in a part of channel field of the carrier pocket 25 upper part, and a high electric-field field is formed in the remaining part of a channel field. At this time, a drain current flows in the source of MOS transistor 112, and as a drain voltage-current property is shown in drawing 8 , saturation characteristics are shown according to threshold voltage. Thereby, as shown in drawing 5 (a), the 2nd Rhine memory Lmn is charged. Source potential will rise as charge progresses, and a drain current will not flow in the place where source potential became equal to threshold voltage. Thereby, charge is completed and the noise voltage (VoutN) which originated in the 2nd Rhine memory Lmn at the residual charge by the optical generating charge is memorized.

[0065] The 2nd switching circuit CK2 and precharge switching circuit CK6 are opened after termination of a blanking period. Subsequently, although it returns at an are recording period, while performing are recording actuation at this time, actuation which outputs the electrical potential difference of the difference of the source potentials VoutS and VoutN memorized by the Rhine memory Lms and Lmn is performed. The actuation which outputs source potential to below is explained.

[0066] That is, 3rd switching circuit CK3 and 4th switching circuit CK4 are closed, and the source potentials VoutS and VoutN which both the Rhine memory Lms and Lmn was made to memorize are made to input into the 1st negative input terminal and plus input terminal of an operational amplifier 31, respectively. At this time, both the reset switch circuits RSTs and RSTn are opened wide. Thereby, the charge of each Rhine memory Lms and Lmn moves to each feedback capacitors Cfs and Cfn, and -VoutS and -VoutN output it to forward [of the 1st operational amplifier 31], and a negative output terminal, respectively.

[0067] This -VoutS and -VoutN are inputted into the 2nd negative input terminal and forward output terminal of an operational amplifier 32, respectively, and the electrical potential difference (VoutS-VoutN) of the difference of VoutS and VoutN is outputted from the output terminal of the 2nd operational amplifier 32. Thus, the video signal (Vout=VoutS-VoutN) proportional to an optical exposure can be taken out.

[0068] As mentioned above, since the insulated gate field effect transistor 112 for lightwave signal detection of the threshold modulation mold which forms the high concentration buried layer 25 in the bottom of a channel as an insulated gate field effect transistor for lightwave signal detection in a pixel, and accumulates an optical

generating charge in the bottom of a channel is used according to the gestalt of implementation of this invention, channel length is long. For this reason, since the electric field from the drain fields 17a and 17b are also eased, a drain induction barrier fall (DIBL) is controlled. Therefore, since the threshold shift is small, as a result fluctuation of a subthreshold level current is also small, the charging current can be minimized. Thereby, since the potential fall by parasitism resistance of wiring etc. can be controlled, direct connection with a capacitive load is attained.

[0069] Moreover, although the time amount of finite is needed for the writing to the Rhine memory Lms and Lmn, the write-in time amount to the Rhine memory Lms and Lmn is sharply short as compared with a blanking period or a read-out period. For this reason, the writing to the Rhine memory Lms and Lmn can be performed into a blanking period etc. By the way, although it will go into the Rhine memory which those parasitic capacitance should read at juxtaposition if two or more Rhine memory is arranged in juxtaposition, the 1st and 2nd source potentials which the Rhine memory which should be read was made to memorize are outputted through a swicthed capacitor circuit. At this time, in a swicthed capacitor circuit, since charge transfer is performed by the 1st operational amplifier 31, the parasitic capacitance seen from the output side of a swicthed capacitor circuit becomes small.

[0070] For this reason, it reads, even if it arranges two or more Rhine memory in juxtaposition, and a rate is hardly influenced. Moreover, since the effect of parasitic capacitance is small, there is also an advantage that the maximum gain is acquired. Moreover, a carrier can be more certainly swept out with low supply voltage by connecting the pressure-up scanning circuit 122 to the source field of MOS transistor 112 for lightwave signal detection.

[0071] Moreover, switching circuit CK7 for a high-voltage block is put in between 1st switching circuit CK1 and 2nd switching circuit CK2, and the source field of MOS transistor 112 for lightwave signal detection. By making connectionless both between 1st switching circuit CK1 and source fields and between 2nd switching circuit CK2 and source fields at the initialization period which impresses the high electrical potential difference for making the optical generating charge accumulated in the high concentration buried layer 25 sweep out Even when the transmission gate which consists of a CMOS transistor as [both] 1st switching circuit CK1 and 2nd switching circuit CK2 is used, malfunction of a transmission gate can be prevented.

[0072] Furthermore, in a series of processes of are recording actuation-read-out actuation-******** (initialization actuation), when an optical generating hole moves, the ideal photo-electric-conversion device which does not interact with the noise source

in a semi-conductor front face or a channel field can be realized. As mentioned above, although the gestalt of operation explained this invention to the detail, the range of this invention is not restricted to the example concretely shown in the gestalt of the above-mentioned implementation, and modification of the gestalt of the above-mentioned implementation of the range which does not deviate from the summary of this invention is included in the range of this invention.

[0073] For example, although it has switching circuit CK7 for a high-voltage block with the gestalt of the above-mentioned operation on perpendicular output line 20a of this side which branches, respectively to the direction of the 1st Rhine memory Lms and the 2nd Rhine memory Lmn as shown in drawing 2 As shown in drawing 6 On branching wiring which branched to the direction of the 1st Rhine memory Lms and the 2nd Rhine memory Lmn from perpendicular output line 20a linked to the source field of MOS transistor 112 for lightwave signal detection, respectively 1st switching circuit CK8 for a high-voltage block And 2nd switching circuit CK9 for a high-voltage block may be formed.

[0074] In this case, it becomes the drive approach as shown in drawing 7 . That is, in a read-out period, 1st switching circuit CK8 for a high-voltage block is closed, the 1st Rhine memory Lms and source field are connected, 2nd switching circuit CK9 for a high-voltage block is closed at a blanking period, and the 2nd Rhine memory Lmn and source field are connected. In both initialization periods, the 1st and 2nd switching circuits CK8 and CK9 for a high-voltage block are opened, and both between the 1st Rhine memory Lms and source fields and between the 2nd Rhine memory Lmn and source fields are made connectionless.

[0075] moreover -- the gestalt of the above-mentioned operation -- the inside of the epitaxial layer 12 of n mold on the substrate 11 of p mold -- the 1st and 2nd wells -- although Fields 15a and 15b are formed -- instead of [of the epitaxial layer 12 of n mold] -- the epitaxial layer of p mold -- n mold impurity -- introducing -- n mold -- a well -- a layer -- forming -- this n mold -- a well -- the inside of a layer -- the 1st and 2nd wells -- Fields 15a and 15b may be formed.

[0076] furthermore -- although various modifications can be considered as structure of a solid state image sensor where this invention is applied -- the MOS transistor for [whatever other structures] light-receiving diode and lightwave signal detection -- adjoining -- a unit pixel -- constituting -- and the well of p mold under the channel field of an MOS transistor -- it is in a field and the high concentration buried layer (carrier pocket) should just be prepared near the source field.

[0077] Furthermore, although the substrate 11 of p mold is used, the substrate of n mold

may be used instead. In this case, what is necessary is just to reverse all of each class explained with the gestalt of the above-mentioned implementation etc., and the conductivity type of each field, in order to acquire the same effectiveness as the gestalt of the above-mentioned implementation. In this case, the carrier which should be accumulated in the carrier pocket 25 is an electron among an electron and an electron hole.

[0078]

[Effect of the Invention] As mentioned above, since the insulated gate field effect transistor for lightwave signal detection of the threshold modulation mold which prepares a high concentration buried layer in the bottom of a channel as an insulated gate field effect transistor for lightwave signal detection in a pixel, and accumulates an optical generating charge in the bottom of a channel is used according to this invention, channel length is long.

[0079] For this reason, since fluctuation of threshold voltage is small, as a result fluctuation of a subthreshold level current is also small, the charging current can be minimized. Thereby, since the potential fall by parasitism resistance of wiring etc. can be controlled, direct connection with a capacitive load is attained. Moreover, in a swicthed capacitor circuit, although the 1st and 2nd source potentials which the Rhine memory which should be read was made to memorize are outputted through a swicthed capacitor circuit, since charge transfer is performed by the 1st operational amplifier, even when two or more Rhine memory is arranged in juxtaposition, the parasitic capacitance seen from the output side of a swicthed capacitor circuit becomes small. For this reason, it reads, even if it arranges two or more Rhine memory in juxtaposition, and a rate is hardly influenced, and the maximum gain is acquired.

[0080] Moreover, since the switching circuit for a high-voltage block is put in between the preceding paragraph of a signal output circuit, i.e., the 1st switching circuit, the 2nd switching circuit, and the source field of the insulated gate field effect transistor for lightwave signal detection, even when the transmission gate which consists of a CMOS transistor as [both] the 1st switching circuit and 2nd switching circuit is used, malfunction of a transmission gate can be prevented at the initialization period when the high voltage is impressed to a source field.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is drawing showing the circuitry of the whole solid state camera concerning the gestalt of operation of this invention.

[Drawing 2] It is the circuit diagram showing the detail configuration of the signal output circuit of the solid state camera of drawing 1 .

[Drawing 3] It is the circuit diagram showing the detail configuration of the Rhine memory part of the signal output circuit of drawing 2 .

[Drawing 4] It is a timing chart at the time of operating the solid state camera of drawing 1 .

[Drawing 5] (a) is a timing chart in a read-out period among a series of timing charts at the time of operating the signal output circuit of drawing 2 , and this drawing (b) is a timing chart in a blanking period.

[Drawing 6] It is the circuit diagram showing the detail configuration of the Rhine memory part of the signal output circuit concerning the gestalt of other operations of this invention.

[Drawing 7] (a) is a timing chart in a read-out period among a series of timing charts at the time of operating the signal output circuit of drawing 6 , and this drawing (b) is a timing chart in a blanking period.

[Drawing 8] It is the top view showing the component layout in the unit pixel of the solid state image sensor used for the solid state camera concerning the gestalt of operation of this invention.

[Drawing 9] (a) is a sectional view showing the structure of the component in the unit pixel of the solid state image sensor used for the solid state camera concerning the gestalt of operation of this invention which meets the A-A line of drawing 8 . (b) is drawing showing the situation of the potential in the condition that the optical generating hole was accumulated in the carrier pocket, induction of the electron was carried out to the channel field, and the reversal field is generated.

[Drawing 10] It is the graph which shows the drain current-voltage characteristic of the MOS transistor for lightwave signal detection of the solid state image sensor used for the solid state camera concerning the gestalt of operation of this invention.

[Drawing 11] (a) is drawing showing the circuitry of the whole solid state camera concerning the conventional example, and (b) is a timing chart at the time of operating the solid state camera of (a).

[Description of Notations]

15a the 1st well -- a field

15b the 2nd well -- a field
15c Channel dope layer
16a A low-concentration source field
16b A high-concentration source field (contact layer)
17 Impurity Range
17a A low-concentration drain field
17b A high-concentration drain field (contact layer)
18 Gate Dielectric Film
19 Gate Electrode
20a, 20b Perpendicular output line
21a, 21b VSCAN supply line
22a, 22b VDD supply line
25 Carrier Pocket (High Concentration Buried Layer)
26 Water Hiraide Line of Force
27a, 27b HSCAN supply line
30a, 30b Pressure-up electrical-potential-difference supply line
31 1st Operational Amplifier
32 2nd Operational Amplifier
101 Unit Pixel
102 VSCAN Drive Scanning Circuit
103 VDD Drive Scanning Circuit
104 HSCAN Input Scanning Circuit
105 Signal Output Circuit
107 Video-Signal Output Terminal
108 Pressure-Up Scanning Circuit (High-Pressure-Distribution Circuit)
111 Light-receiving Diode
112 Insulated Gate Field Effect Transistor for Lightwave Signal Detection (MOS Transistor for Lightwave Signal Detection)
CK1 The 1st switching circuit
CK2 The 2nd switching circuit
CK3 The 3rd switching circuit
CK4 The 4th switching circuit
CK5, CK6 Precharge switching circuit
CK7 Switching circuit for a high-voltage block
CK8 1st switching circuit for a high-voltage block
CK9 2nd switching circuit for a high-voltage block

Lms 1st Rhine memory (the 1st memory)
Lmn 2nd Rhine memory (the 2nd memory)
RSTs, RSTn Reset switch circuit

[Translation done.]